Rohith Prakash

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github.com/rnprakash

Expertise

Machine learning: Optimization; design of supervised classification and regression algorithms; model building; design of unsupervised similarity algorithms; Bayesian inference; probabilistic hashing **4+ years**

Systems & Security: Microarchitectural design of secure systems; building anomaly detectors; quantifying privacy and leakage **4+ years**

Education

UT Austin May 2018
Masters in Computer Engineering GPA: 3.7
Advisor: Prof. Mohit Tiwari

UT Austin May 2014
B.S. in Computer Engineering GPA: 3.7
Senior project: "TEx86: A FAST Simulator for Processor Design Architects"
Advisor: Prof. Derek Chiou

UT Austin May 2014
B.S. in Mathematics GPA: 3.5
Topic: Pure Mathematics

Research Interests

Security & Privacy: Anomaly detection; machine learning and optimization; differential privacy; side-channel attacks; inference attacks; OS- and systems-level defenses

Computer Architecture: Memory and cache systems; hardware support for private microarchitectural queues

Work and Research Experience

UT Austin Aug 2014— *Current*
Graduate Research Assistant

Optimization of attacker models for side-channel attacks using machine learning. Use of information theoretic concepts to demonstrate and quantify the potential for information leakage.
Thwarting queue contention channels with differential privacy. Creation of a generic queue architectural structure which can be tuned to give variable privacy guarantees with speed trade-offs.
Design of cross-stack anomaly detector using a novel behavioral-hashing algorithm. Normal behavior is learned by analyzing interactions across the stack. Behavioral-hashing algorithm efficiently transforms observations to lower-dimensional hash values to efficiently identify similarities in behavior.

ARM May 2017–Dec 2017
Graduate Research Intern

Behavioral hashing for optimal prefetcher utilization. Introduce behavior-sensitive hashing to design of an adaptive, dynamic meta-prefetcher. Prefetcher selectively enables or disables existing prefetchers based on memory stream behavior.

Altera Corp. May 2015–Aug 2015
Security Research Intern

Researched, tested, and analyzed various hardware and algorithmic implementations for physical-unclonable functions (PUFs). Given SRAM cells for use in prototype PUFs, analyzed cell data to create algorithms for determining PUF reliability, resilience, enrollment procedures, and bit selection.

UT Austin Aug 2014–Dec 2014
Graduate Teaching Assistant

Teaching assistant for sophomore undergraduate C/C++ class (EE 312: Software Design and Implementation I).

Intel Corp. Jun 2014–May 2015
Graduate Technical Intern

Tested, verified, and debugged camera unit memory interface systems. Compiled models, ran regressions, and debugged synthesized Verilog for Intel Atom processors.

Intel Corp. Feb 2012–Aug 2013
Undergraduate Technical Intern

Performed gate-level simulation (GLS) for the Intel Atom processor. Compiled models, ran regressions, and debugged synthesized Verilog. Created and maintained validation automation tool (written in C, Perl and Tcl/Tk) which allowed validation engineers to automatically build and fix common build errors quickly.

Computer Skills

Languages: C/C++, x86 ISA, Python (Keras, Tensorflow), ARM ISA, Julia, Java, and more

Operating Systems: Linux/Unix-based, Windows

Scholarships and Awards

2014 — Current: Graduate Research and Tuition Grant
Aug 2010 — 2014: Engineering Undergraduate Honors
2012, 2014, 2015: Intel Individual Contributor Award
2015: UTexas Hackathon — Top 10 & Dell Innovation Award

Other

Languages: English, French
Citizenship: US Citizen